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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 3 (canceled)

1
Claim 4 (previously presented): A correlator for performing a communications acquisition, comprising:

a FIFO memory having a memory input and a memory output, said FIFO memory inputting and outputting a content;

a shift register with feedback for holding a received signal sequence in serial form, said shift register having register positions connected in parallel to said memory input for parallel storage of a plurality of shift register contents read out in succession, said memory output being connected in parallel with said register positions for parallel transfer of data to said shift register;

a further memory for holding reference signal sequences; and

a comparator for comparing the content of said FIFO memory with a content of said further memory;

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the correlator programmed to perform the step of:

correlating a binary-coded spread sequence arriving at a frequency f and having m bits with a locally generated spread sequence by

storing the received binary-coded spread sequence;

splitting the stored received binary-coded spread sequence into k sections; and

correlating the sections of the stored received binary-coded spread sequence at a frequency of $k*f$ with corresponding sections of the locally generated spread sequence.

²
Claim ⁵ (original): The correlator according to claim ⁴,
wherein said comparator has a comparator output, and including
an adder comprising two-bit adders configured to form a
cascaded interconnection, each of said two-bit adders having
at least two inputs and an output, said output of each of said
two-bit adders connected to one of said at least two inputs of
a succeeding one of said two-bit adders, said adder connected
to said comparator output and configured to add up logic
values produced during bit-by-bit comparison for matching bit
positions.

Claims 6 - 7 (canceled)